

## IN THE SPECIFICATION

Cancel the revisions made to paragraph 22 via the Amendment submitted 13 June 2002 for revising the Text and, in place of those revisions, amend paragraph 22 as follows:

[0022] Wong et al ("Wong"), "A Wide Tuning Range Gated Varactor," IEEE J. Solid-State Circs., ~~IEEE J. Solid-State Circs.~~, May 2000, pages 773 - 779, describes another type of semiconductor varactor. As generally shown in Fig. 7, Wong's varactor is created from n ~~body n+body~~ region 60 of a semiconductor body. Using somewhat unusual terminology, Wong's varactor includes heavily doped p-type ~~n-type~~ "source" 62 and heavily doped n-type ~~p-type~~ "drain" 64 laterally separated from each other along the upper semiconductor surface. Gate dielectric layer 66 separates gate electrode 68 from moderately doped n-type body material situated between source 62 and drain 64. Wong reports that the varactor capacitance is defined as the capacitance looking into the drain node.

Amend paragraphs 110, 126, and 262 as follows:

[0110] Transition voltage  $V_X$ , the value of plate-to-body bias voltage  $V_R$  at which inversion layer 130 or 180 disappears, is derived in the following manner as a function of gate-to-body voltage  $V_{GB}$ . The derivation of transition voltage  $V_X$  is performed under the general simplifying assumptions employed in Grove, Physics and Technology of Semiconductor Devices ~~Physics and Technology of Semiconductor Devices~~ (John Wiley & Sons), 1967, and does not include quantum-mechanical threshold-voltage corrections typically associated with values of gate dielectric thickness  $t_{GD}$  less than 10 nm. The derivation is done here for the n-channel varactor of Fig. 8 but, with appropriate reversals in voltage polarities, applies to the p-channel varactor of Fig. 10.

[0126] The gate-enhanced junction varactor of the present invention was computer simulated in two dimensions to validate the operational principles and analytical theory. The simulation was conducted on a stripe-type (rectangular) silicon-gate implementation of the n-channel varactor of Fig. 8 using the Medici two-dimensional simulation program. See Medici Two-Dimensional Device Simulation Program User's Manual, ~~Medici Two-Dimensional Device Simulation Program User's Manual~~, version 1998.4, Avant! Corp., 1999.

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[0262] The layout of Fig. 26 provides a tradeoff between quality factor and the minimum achievable value of minimum capacitance  $C_{Vmin}$ , and thus the maximum achievable value of the  $C_{Vmax}/C_{Vmin}$  varactor capacitance ratio, relative to the layout of Fig. 24. The lateral dimension of each finger portion 102F perpendicular to the length of the portion 102F can be chosen in accordance with the minimum feature size of the layout design rules. Nonetheless, because plate region 102 consists of main plate portion 102M and at least one finger portion 102F, the minimum achievable value of plate area  $A_p$  is greater in the layout of Fig. 26 than in the layout of Fig. 24. On the other hand, the presence of one or more finger portions 102F improves the quality factor of the layout of Fig. 26 compared to that of Fig. 24.

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